REMARKS

This paper is filed in response to the office action mailed on 11/5/03. With regard to the objections made to the specification it is submitted that the prior amendments offered to the specification at page 4 are to be made at page 4, not page 3. Per the examiner's request a revised abstract is submitted. A clean copy is attached hereto.

Claims 15-18 are allowed and claims 5-8, 11 and 12 have been objected to, but would be allowable if written in independent form.

Claims 1-4, 9, 10, 13, and 14 have been rejected under section 35 U.S.C. 102(e) as being anticipated by Augusto (6,620,710.) Based on the arguments that follow, it is respectfully submitted that each of the rejected claims is patentably distinct and in condition for allowance.

Applicant's claim 1 requires " ... a monocrystalline third doped region of different conductivity type than the first region,..." In the office action, the examiner characterizes Augusto as disclosing "a monocrystalline third doped region 132" and identifies this as the channel 132 of Figures 40-44.

Augusto's channel 132, however, is disclosed as an undoped film, and is therefore inconsistent with applicant's "third doped region" of claim 1. Augusto teaches, "In a preferred embodiment, the channel 132 is an undoped film..." (col. 15, lines 16-17). This is understood to mean that the channel 132 will at most include a low level of impurities akin to intrinsic semiconductor material. In fact, Augusto clearly states, "Thus, the present invention preferably provides a channel region in which a low concentration (if any) of impurities exist..." See Col. 16, line 38. Therefore, applicant's doped third region cannot be read on Augusto's channel 132.

Moreover, it is submitted that the Augusto reference does not at all teach or suggest thermal processing at the level that would stimulate movement of dopant into channel 132 and, in fact, the reference teaches away from any thermal processing which would diffuse a dopant into the channel 132. At Col. 4, lines 25 to 29, Augusto states,

> "Since the method of the present invention does not produce the channel film until after all the ion implantations and the associated thermal annealing processes have been completed, the channel film is preferably not exposed to the high temperatures of the prior art methods. As a result, undoped materials may be

used as the channel film, ..."

At Col 4, line29 to 30, Augusto further states,

> "Since the present invention preferably does not produce a channel until after the junctions have been formed, the channel region ultimately formed is not affected by impurities introduced by the junction profiles."

Also, at Col 4, line 42 Augusto further states,

> "Since the entire gate stack and the channel under the present invention do not undergo high temperature processing, the channel can be produced with silicon-based alloys."

From all the above citations, it is apparent that Augusto does not contemplate that the region 132 (which examiner attempts to equate to applicant's third doped region) is a region that is doped. Further, if the channel 132 of Augusto, which examiner equates to applicant's claimed "third doped region" were to receive thermal treatment to cause doping of the channel 132, the major source of dopant would clearly be Augusto's region 108, described by the examiner as "the right-most of the two n-type source/drain regions."

The examiner read applicant's first doped region on Augusto's region 108 in order to formulate the rejection. However, even if the doping were to occur, the conductivity-type of the dopant of the third region would clearly become the same as the conductivity-type of the first region and applicant's claim 1 still could not be read on the prior art. This is because claim 1 requires a "third doped region of different conductivity type than the first region ..."

Thus, the Augusto reference does not teach or suggest a "third doped region" of different conductivity type than the first region" and, furthermore, Augusto teaches away from any suggestion to provide for a "third doped region of different conductivity type than the first region." Based on this argument it is submitted that claim 1 is patentably distinct over the art of record and should be allowed.

Claim 9 also requires "a third doped region over the first region of different conductivity type than the first region; ..." For the same reasons that claim 1 is distinct and nonobvious, claim 9 is also allowable over the art.

Each of the dependant claims 2-4, 10, 13 and 14 include subject matter which, in combination with claim 1, add additional patentable distinctions. Reconsideration of claim 2 is also requested because claim 2 provides that the "third region is a channel region of the MOSFET." Again, the channel 132 of Augusto (which the examiner equates to applicant's third doped region) is undoped and, is therefore, inconsistent with applicant's third region. It is respectfully submitted that claim 2 is novel and in form for allowance.

Claim 3 requires that "the second region is a portion of a transistor" and claim 4 requires that the second region is a "second source/drain region associated with a second MOSFET..." and that the "channel region of the second MOSFET" is " aligned with the second source drain." Because these features are required in combination with the "third doped region" of claim 1, it is submitted that they are patentably distinct over the art and should be allowed.

Claims 13 and 14 also include a combination of features which further distinguish the invention. Claim 13 requires that the "conductive layer is a continuous film extending from the first region to the second region." Claim 14 requires that "the conductive layer physically contacts the first region and second region." Each of these requirements in combination with the "third doped region" of claim 1 is absent from the art of record.

For all of the above reasons, it is submitted that the rejected claims are allowable and it is requested that the application be passed to issuance.

Respectfully submitted,

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ASTRACT

An architecture for connection between regions in or adjacent a semiconductor layer. According to one embodiment a semiconductor device includes a first layer of semiconductor material and a first field effect transistor having a first source/drain region formed in the first layer. A channel region of the transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. The device includes a second field effect transistor also having a first source/drain region formed in the first layer. A channel region of the second transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. A conductive layer comprising a metal is positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

In another embodiment a first device region, is formed on a semiconductor layer. A second device region is also formed on the semiconductor layer. A conductor layer comprising metal is positioned adjacent the first and second device regions to effect electrical connection between the first and second device regions. A first field effect transistor gate region is formed over the first device region and the conductor layer and a second field effect transistor gate region is formed over the second device region and the conductor layer.